A Solution of Test, Inspection and Evaluation for Blind Signal Waveform on a Board

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BiTS
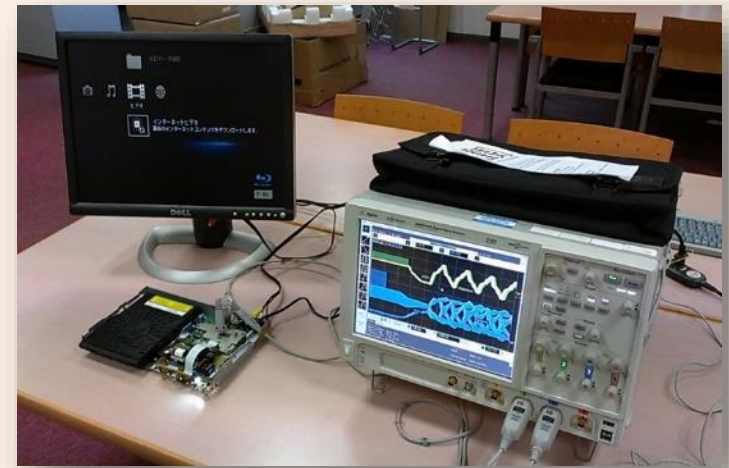Burn-in & Test Strategies Workshop

ELECTRONICS PARTS
SER
CUSTOMIZED SOCKETS & CONNECTORS

Purpose

▶ Blind signal waveform analysis on the system board by using **Signal Probe Socket.**

Conclusion

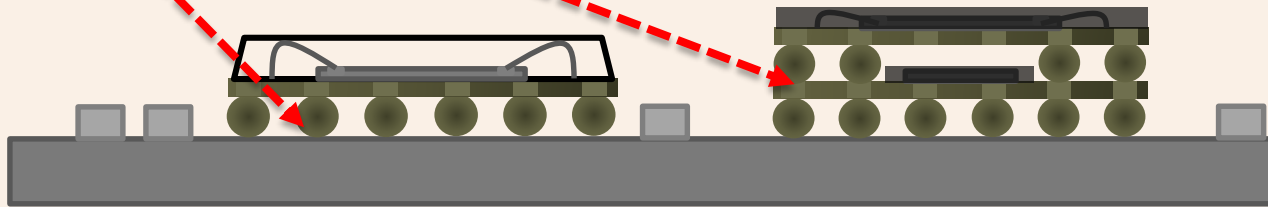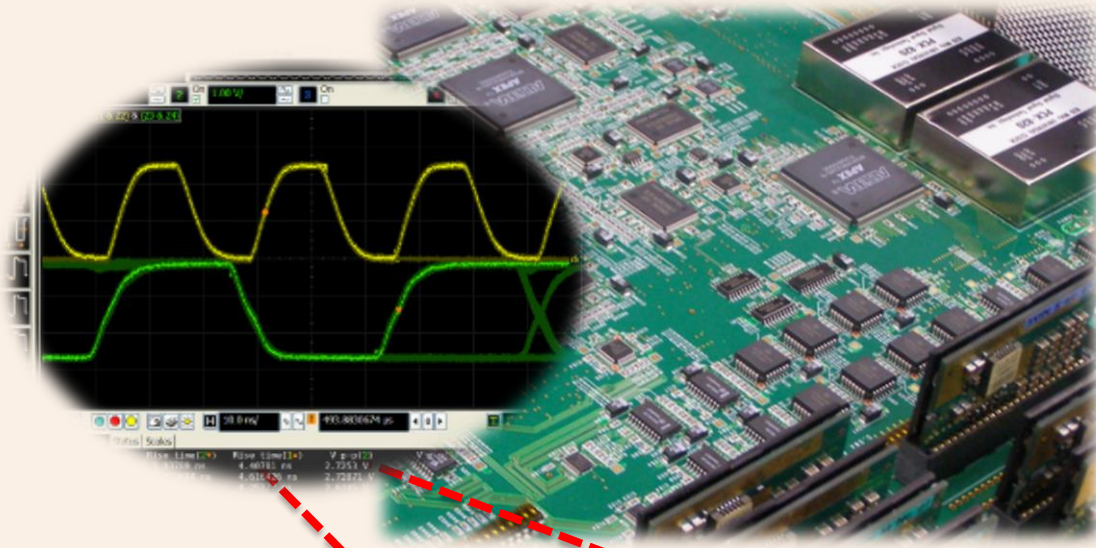▶ Got a real signal waveform by introduction S-parameter data of signal probe socket and **InfiniiSim** performance.

Agenda

1) What is a blind signal analysis?

2) Signal probe socket !

   2-1) YOROI ???

3) Blind signal measurement & data

4) Conclusion & summary

1) What is a blind signal analysis ?

Blind Signal !

Blind signal analysis !

- ■ Timing analysis between DDR and CPU.
- ■ Measure and confirm a blind signal waveform directly underneath IC package.
- ■ Define different approach for identification of a failure point when not re-appearance on LSI tester.
- ■ Qualification of memory and CPU.
- ■ Moving measurement point by using InfiniiSim.

Timing signal & waveform

Timing analysis
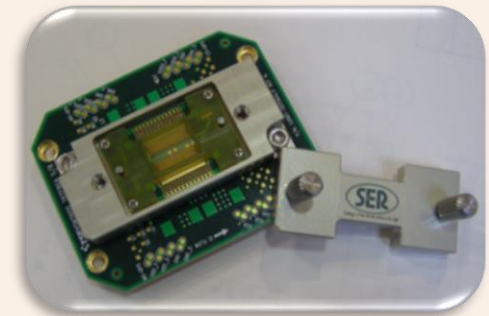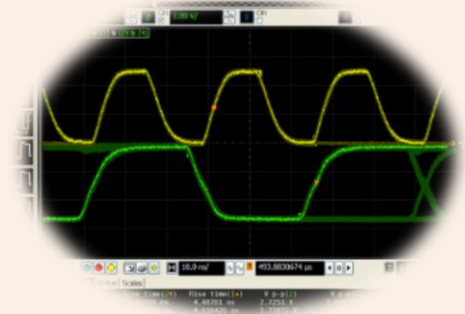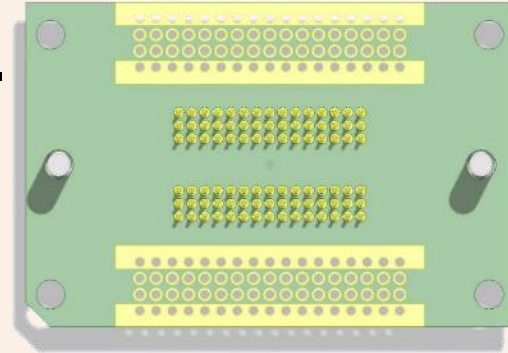Verification
Quality control
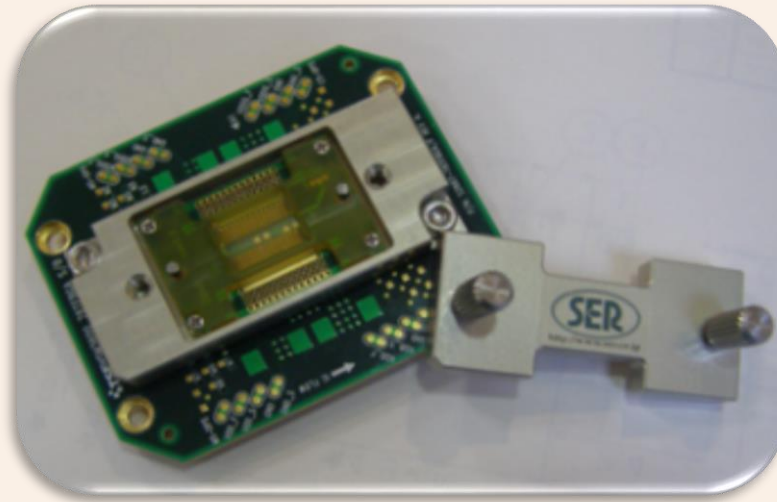

DDR Clock

Hold Time

Write and Read waveform

Set up Time

Blind signal measurement

1. **All signals** of 0.8mm pitch device should be accessible for measurement.

2. Support of **high- speed** signal measurements over 3.5 Gbps.

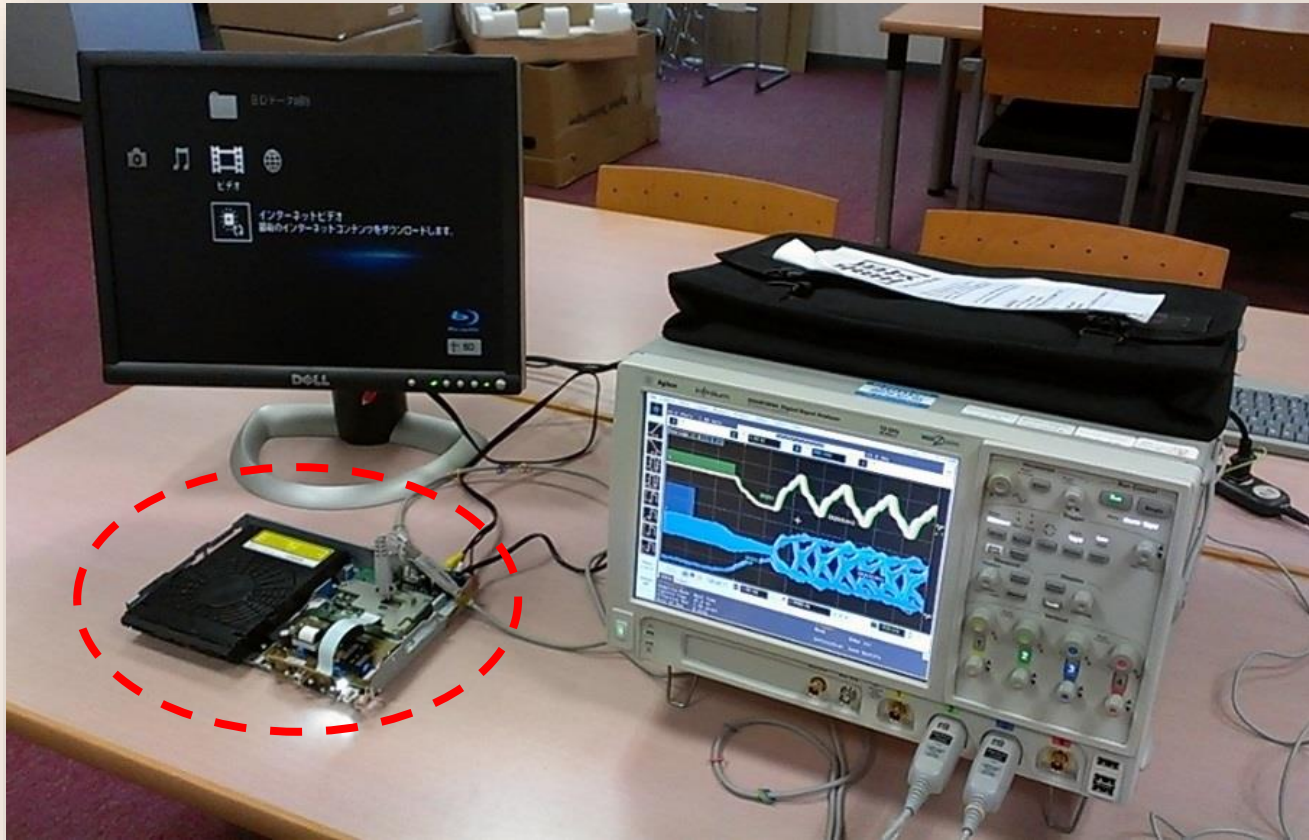3. **Solderless mount.**

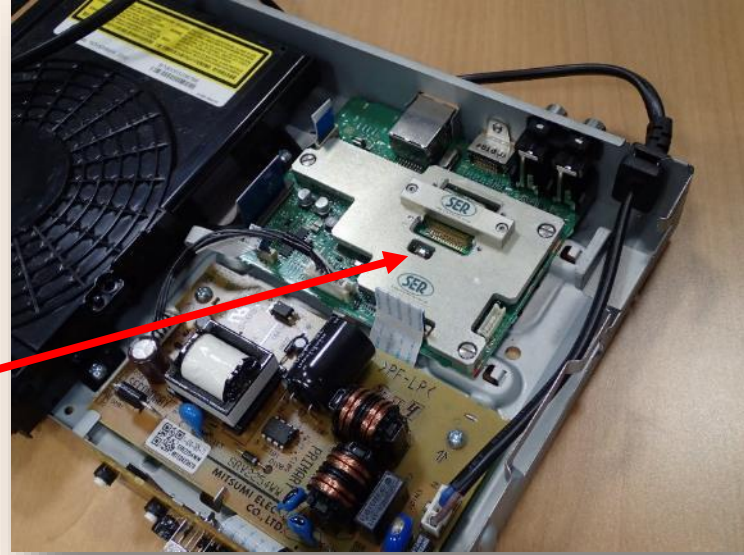   (Easy to replace the target IC)
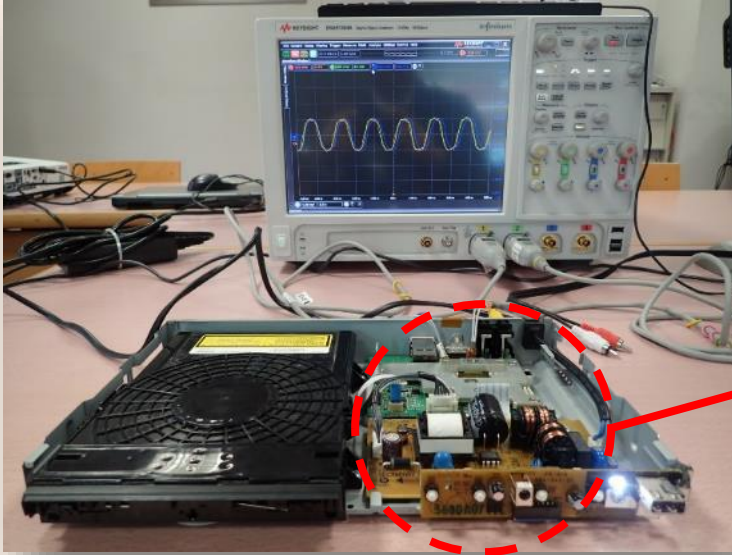
2) Signal Probe Socket !

Blind signal probing

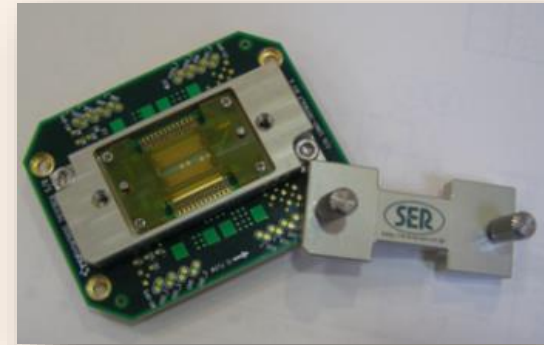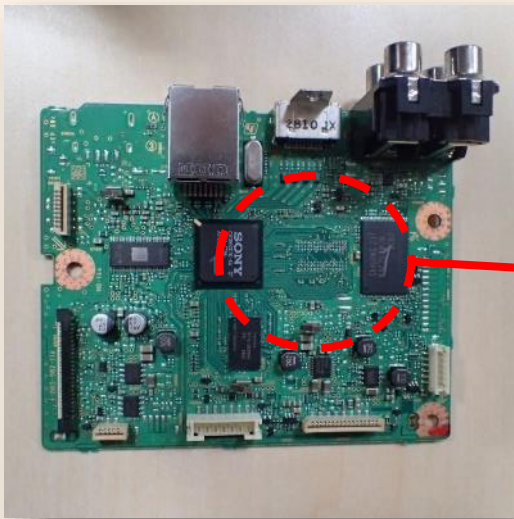## Signal measurement on DVD player

Blind signal probing

Signal probe socket is on a board of DVD player and connected to the oscilloscope.
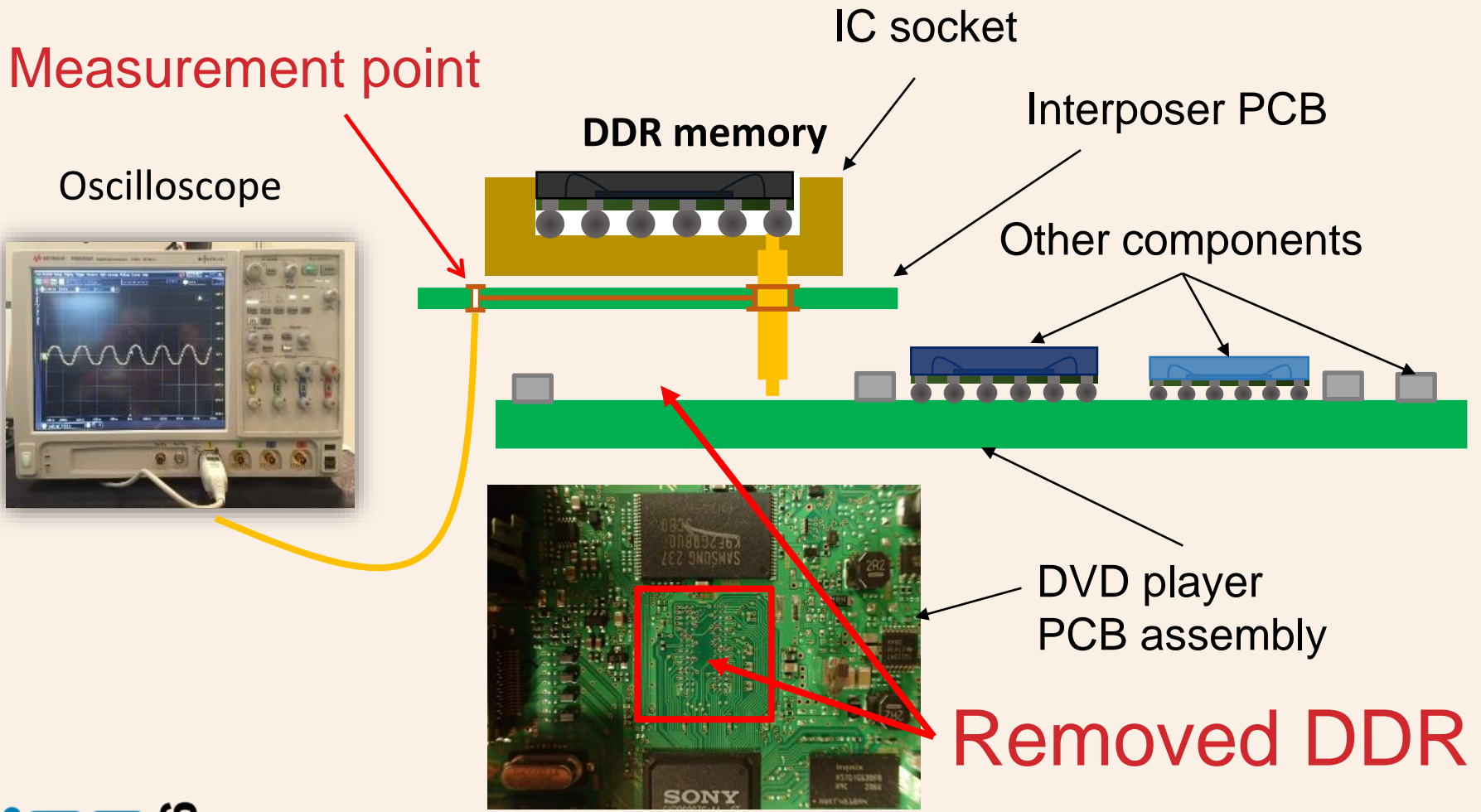
Blind signal probing

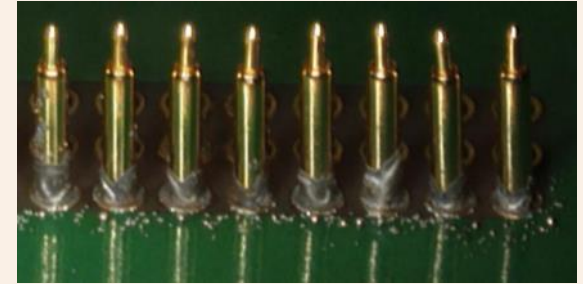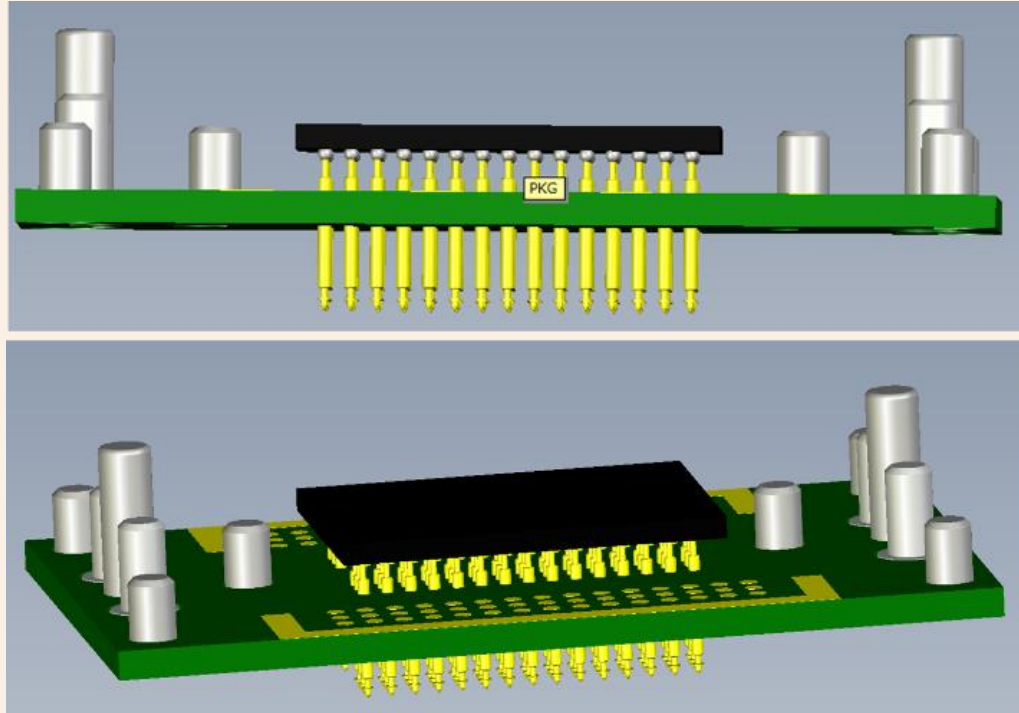Removed DDR memory and mounted signal probe socket worn YOROI.

Setup for DDR memory's blind signal measurement

Measurement point

IC socket

DDR memory

Interposer PCB

Oscilloscope

Other components

DVD player
PCB assembly

Removed DDR

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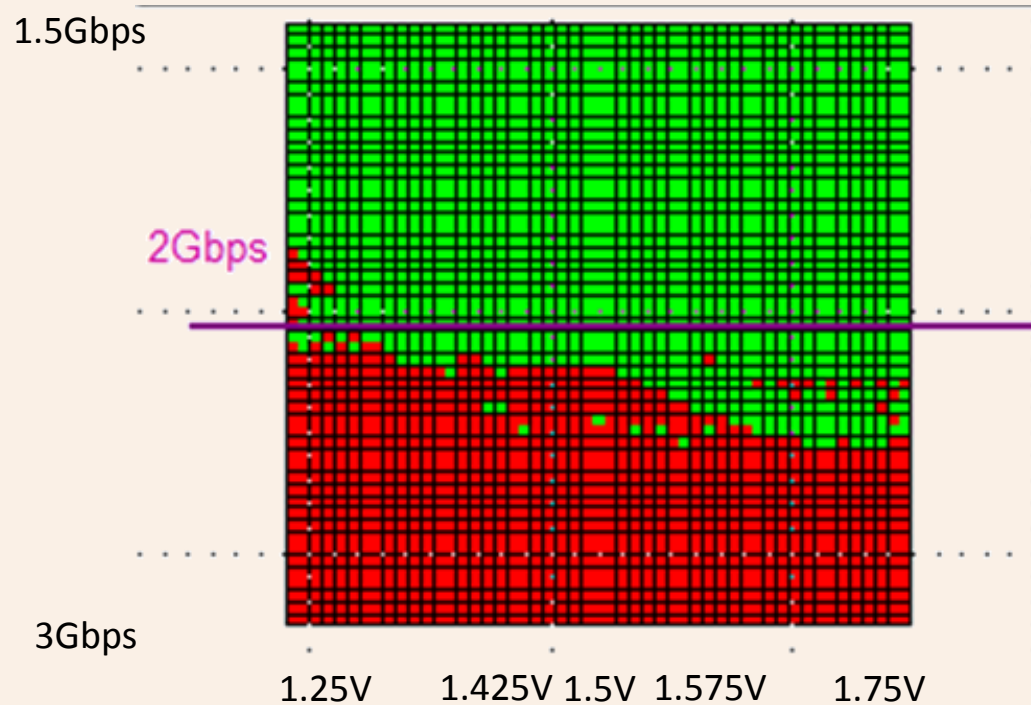# Signal probe socket basic structure

Example
PKG: BGA (DDR3 memory)
Pitch: 0.8mm
Pin count: 96 pin

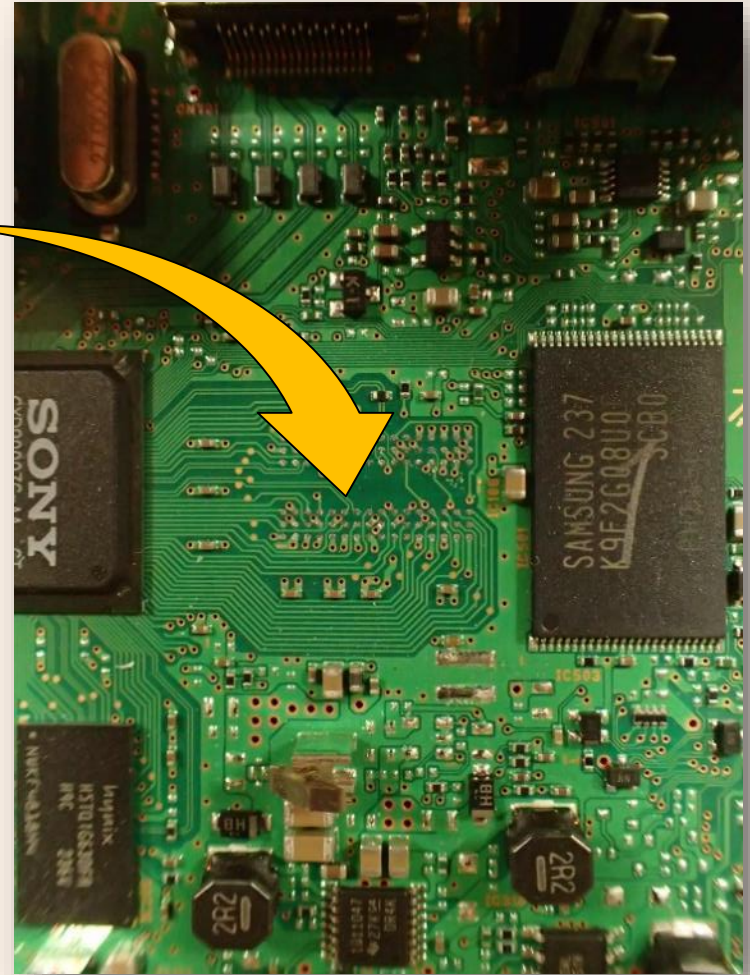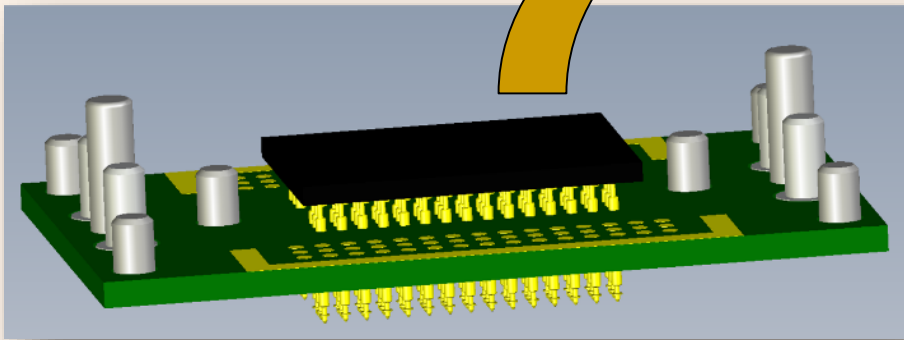# Actual performance of DDR memory's signal probe socket

Shmoo plot analysis result

Tester
-Verigy
-V93000
-HSM3600

Blind signal probing design structure

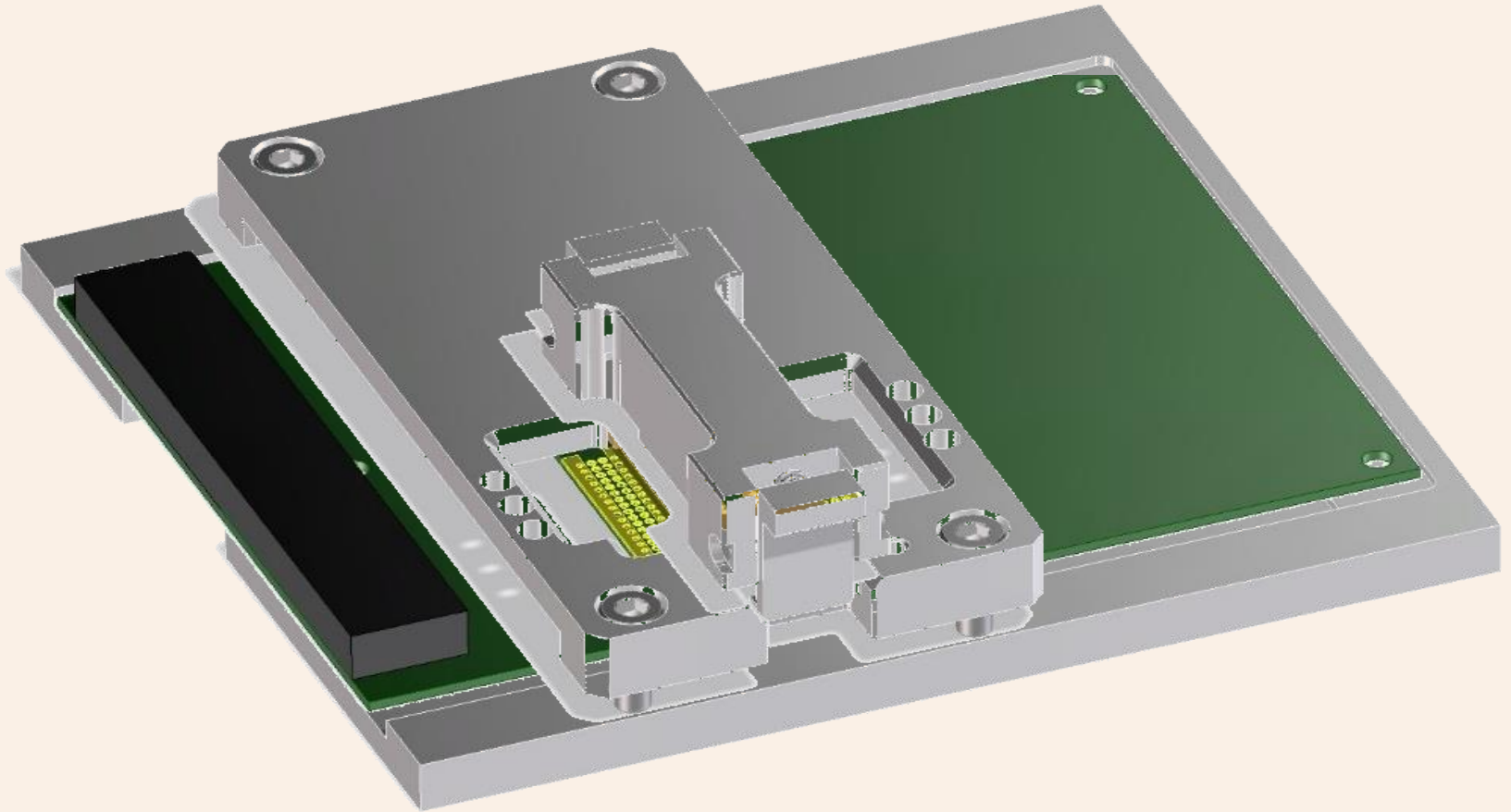YOROI structured mount is required for signal probe socket

2)-1 YOROI ???

SAMURAI wore YOROI for fighting.
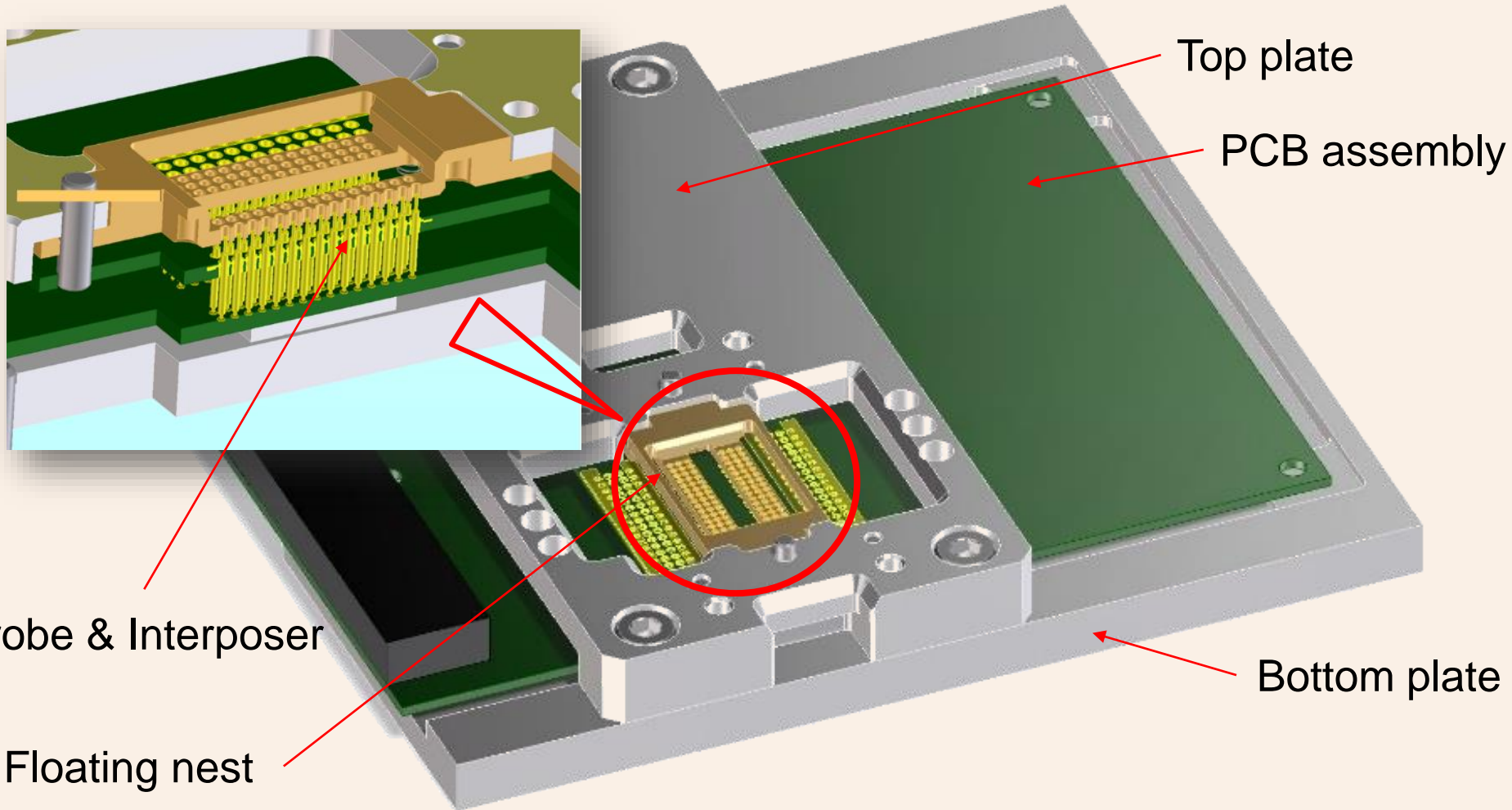
And signal probe socket also must be.

Why ?

YOROI structure for signal probe socket

(Patent pending)

Signal probe socket worn YOROI

Top plate

PCB assembly

Probe & Interposer

Floating nest

Bottom plate

(Patent pending)

Interposer element

It influences the measurement of the blind signal waveform.

Directly underneath the ball (real signal)

· Waveform measured directly underneath the ball

· Waveform at measurement point

Equivalent circuit model

PCB

L   C

Interposer pattern for measurement (stub)
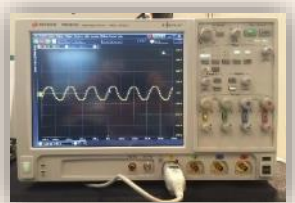
3) Blind signal measurement & data

Testing procedure & method

Target is this signal waveform
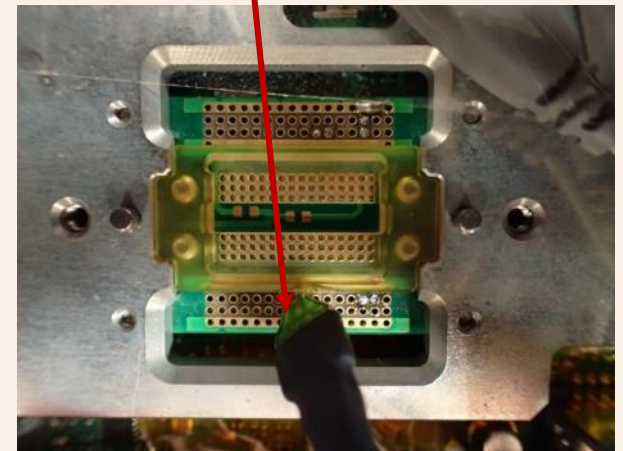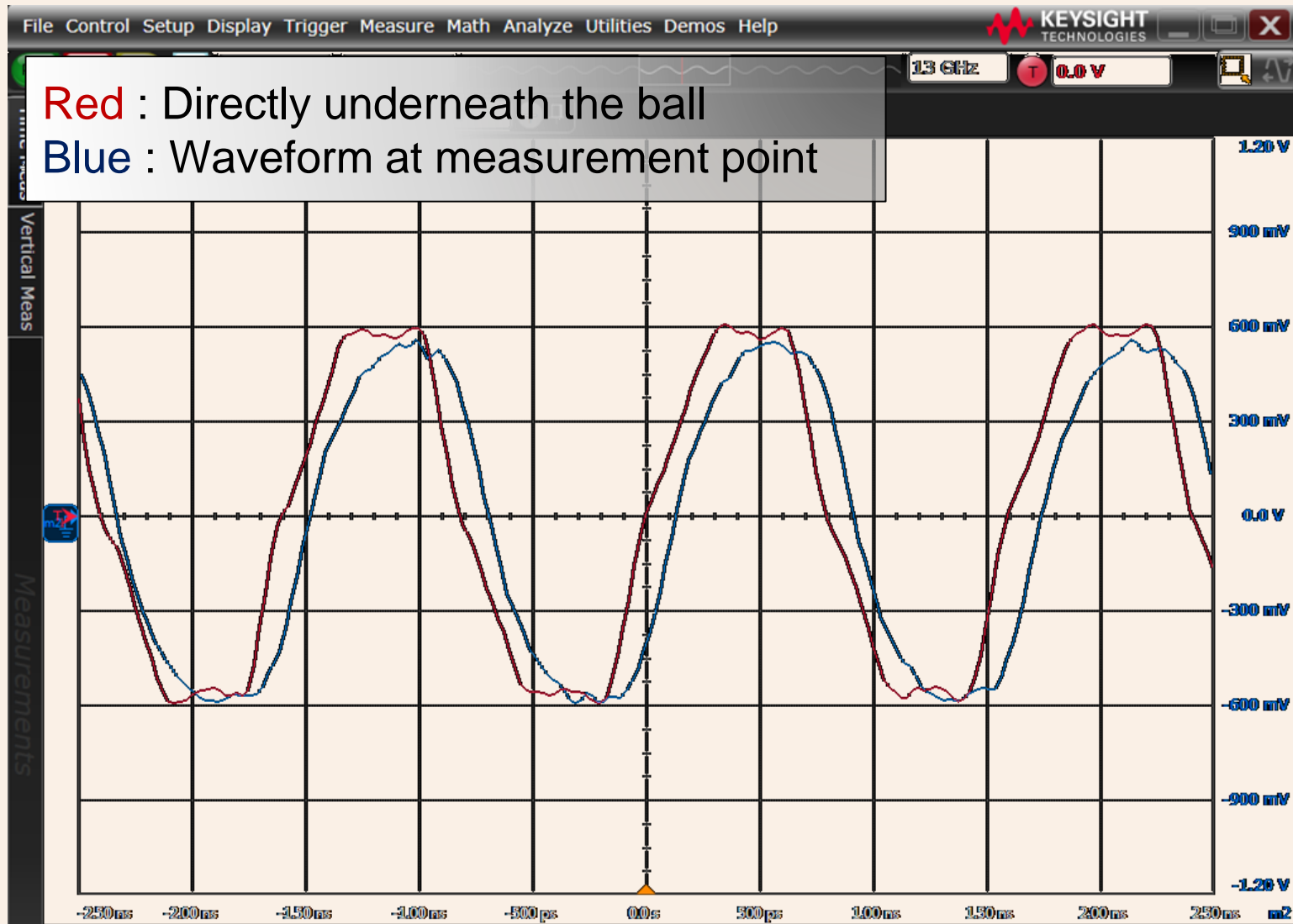
DDR Memory

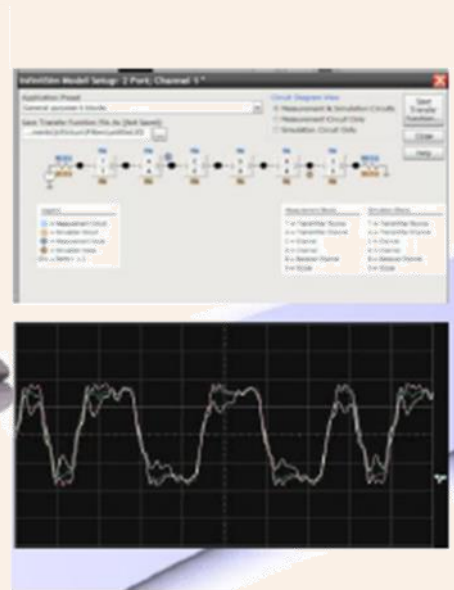Measurement point on interposer

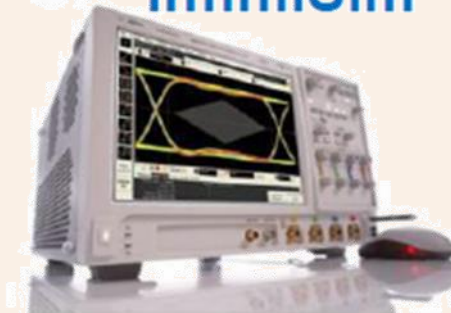Measurement point

DDR Memory
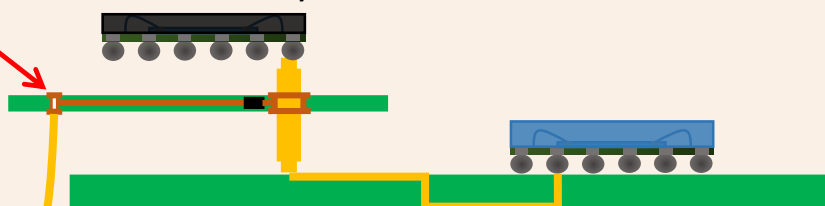
Actual DDR clock signal waveform

Waveform transformation

InfiniiSim by Keysight Technologies

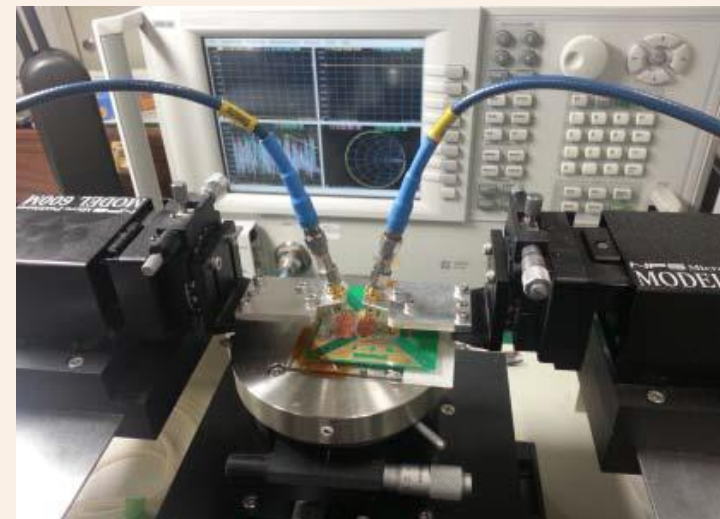# S-parameters of signal probe socket

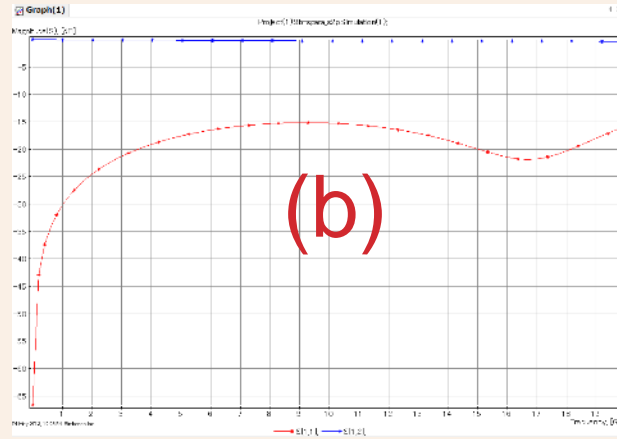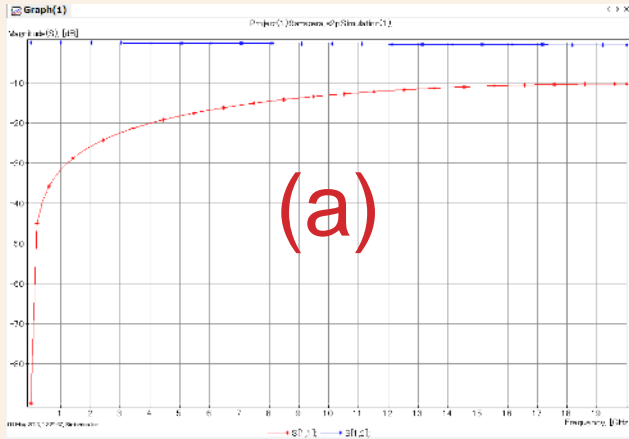Actual S-parameter data of signal probe socket
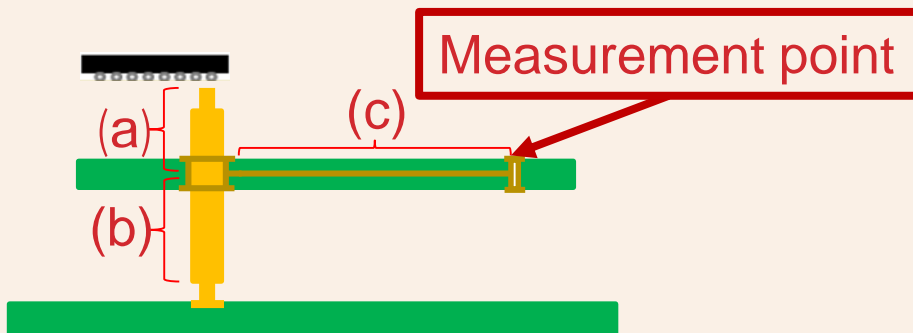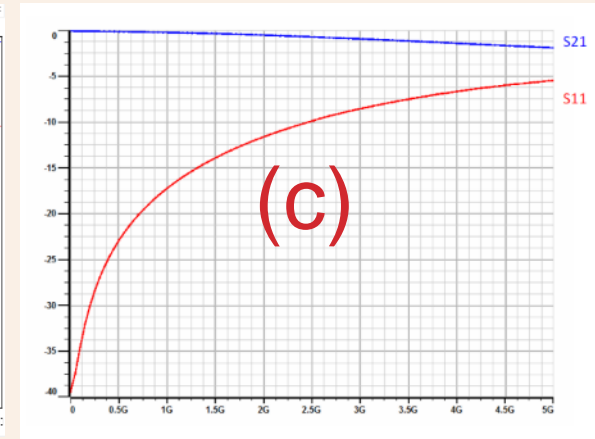
Waveform transformation

Measurement point waveform includes
all S-parametric data of (a),(b) and (c)

(a),(b) and (c) must be subtracted from
measurement waveform to get the actual
data of the IC terminal.

Waveform transformation

DUT   Ball/Pad

(a)
(c)
(b)
PCB Pad

Testing procedure & method

Test point directly underneath the ball

DDR Memory

Measurement point

DDR Memory

Measurement point on interposer

DDR Memory

Measurement point after using InfiniiSim transformation

Moving measurement point
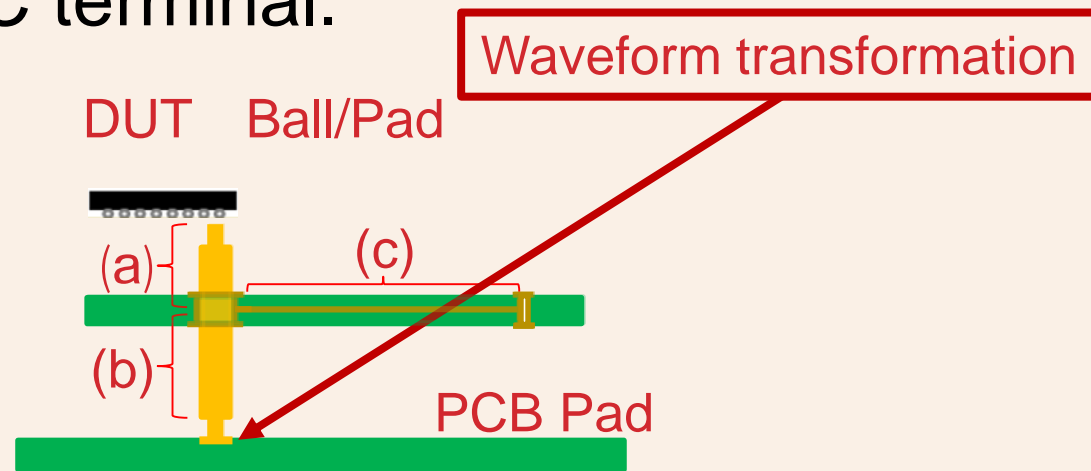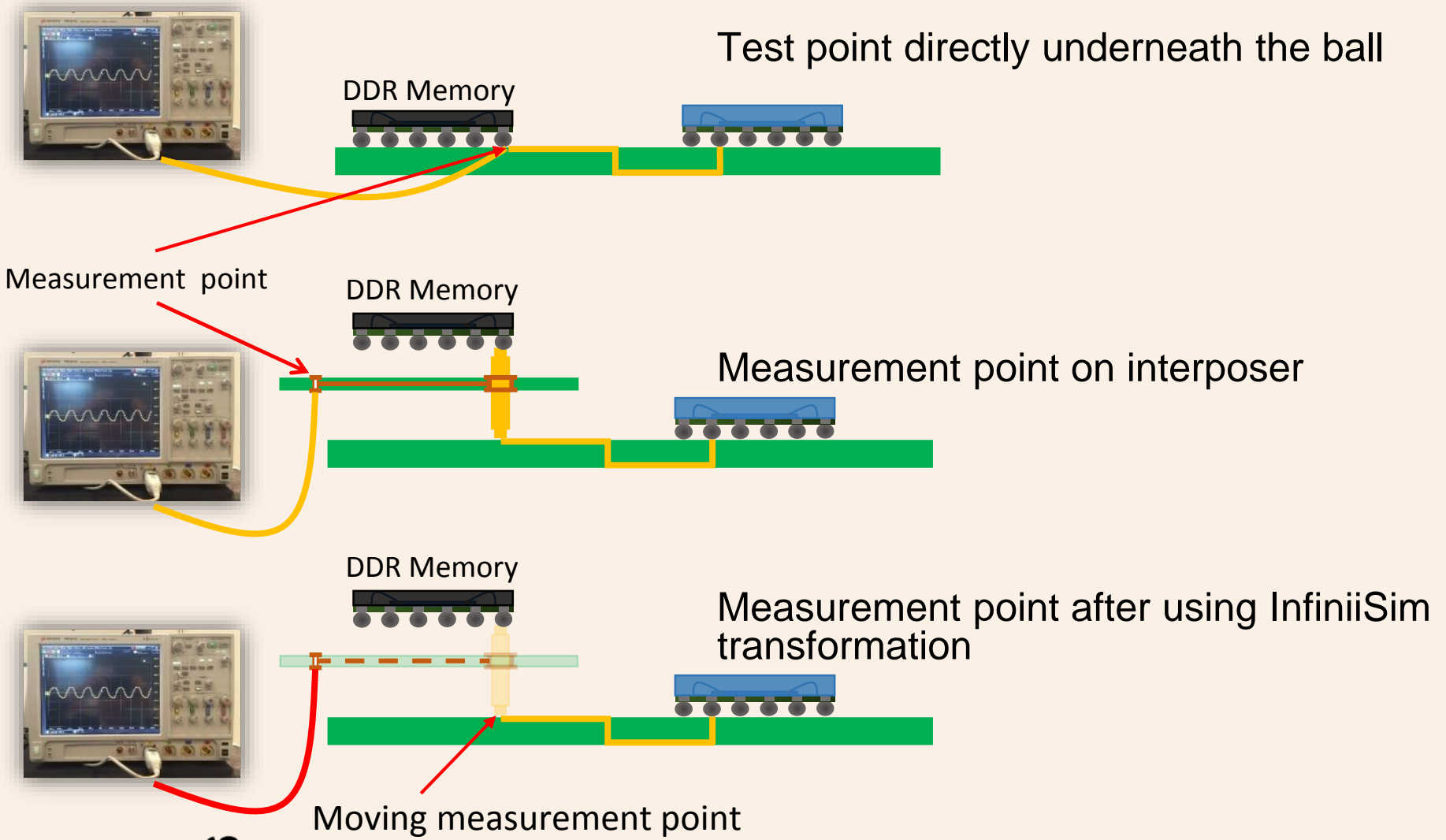
DDR clock signal waveform transformed

Red : Directly underneath the ball
Blue : Waveform at measurement point
Green : Waveform after transformation by InfiniiSim
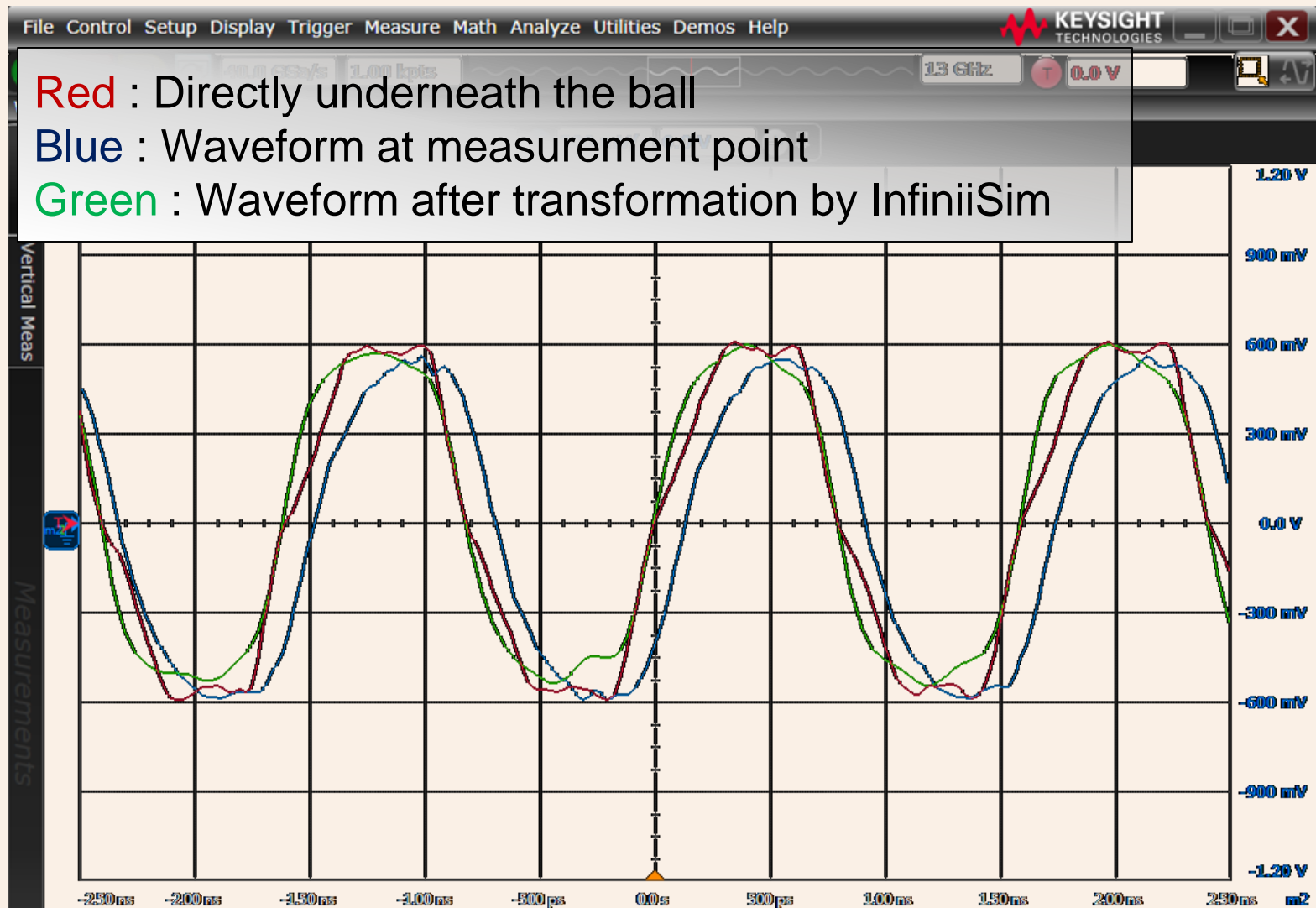
4) Conclusion & Summary

Conclusion & Summary

1. The signal probe socket can measure blind signal waveform behind of IC package.

2. Blind signal waveform is able to reform by InfiniiSim using S-parameter data of signal probe socket.

3. It bring system engineers significant system performance information detail.

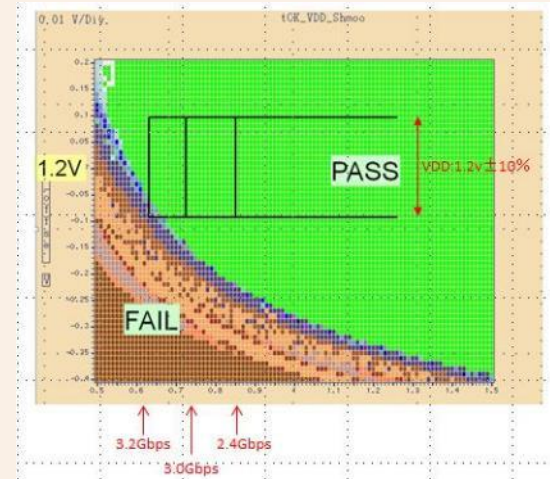4. It is a new approach for evaluation & analysis in the world.

Future works

1. Support high speed **DDR4** memory

   Minimize stub

   Minimize probe length

   4.3mm ⇒2.6mm

   And for 10GHz speed requirement

2. Approach **power integrity** analysis

Acknowledgements
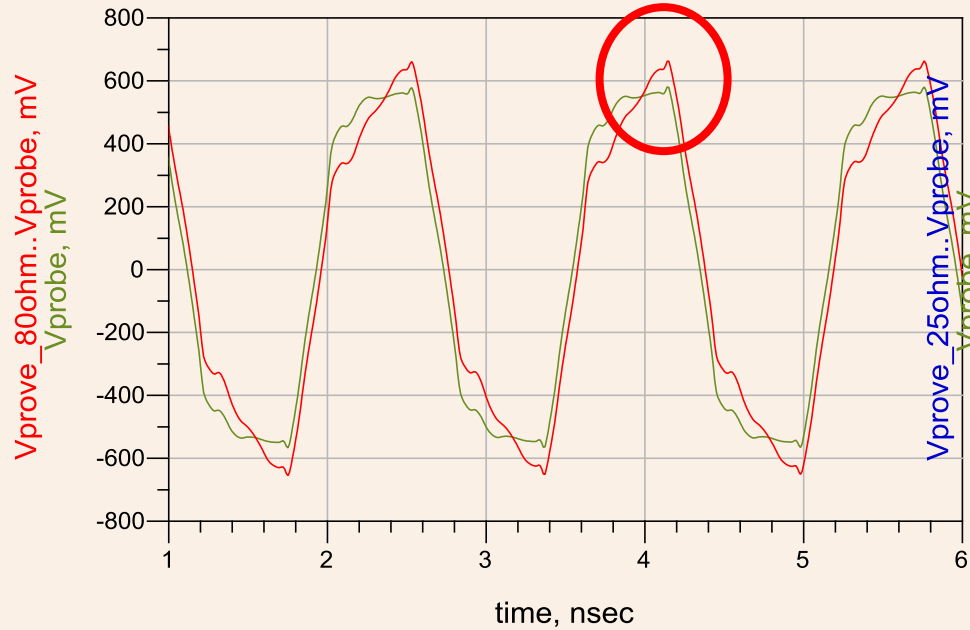
Keysight Technologies Japan

Hiroyuki Shimada（MoDech inc)

Appendix